Clean Version of Changes to Specification

Please replace the paragraph at page 2, lines 1-15 with the following paragraph.

Design of storage devices and processes for their fabrication have become quite sophisticated and have resulted in very low process cost for fabrication and very small memory cell area. Therefore it is currently practical to form even relatively large numbers of storage cells together with digital signal processing circuitry on a single chip. Moreover, use of multi-port memories for communication between functional components on a chip has proven to be extremely fast and efficient and thus has come into relatively widespread use. These memories are generally referred to as embedded memories when included with circuits having other than a storage function on an integrated circuit chip.

a4

Please replace the paragraph starting at page 2, lines 16-32 and continuing at page 3, lines 1-4 with the following paragraph

Nevertheless, memory sells, particularly of the dynamic type which store data capacitively, are relatively delicate devices and may be subject to damage or deterioration during manufacture or after being placed in service. When such devices are used for communication and data transfer among functional regions or components, the reliability of storage devices becomes extremely critical to the proper operation of the entire chip. Therefore, it is desirable to test storage cells at different stages of manufacture, board assembly and during system operation. This test is done periodically or at certain system operating states such as power-up of the chip in order to ascertain operability of the memory structures. It is also desirable to provide for broader testing of the various functional elements of the system operating together. Such tests are generally referred to as system level tests by cannot generally be performed by programmable memory BIST arrangements as will be discussed below.

a5

Please replace the paragraph at page 3, lines 5-18 with the following paragraph

Nevertheless, system failures may be attributed to damage caused by external elements, minor manufacturing imperfections and/or aging of the materials, Damage from external elements could impact the correct functioning of an electronic system or any part thereof at any time during its useable life. However, minor manufacturing imperfections are the main cause of system failures at early stages of system operation while aging is the dominant cause of system failures at later stages of the time of the system. For high reliability and availability applications such as banking and medical applications, it is essential to perform periodic testing of system modules.

a6

Please replace the paragraph at page 10, lines 3-14 with the following paragraph

Referring now to the drawings, and more particularly to Figure 1, there is shown a high-level block diagram of an exemplary architecture of a programmable memory BIST module. (It should understood that the depiction of Figures 1-3 are arranged to convey an understanding of the invention and are not admitted to be prior art as to the present invention.) Central to this architecture is a programmable memory BIST controller 10 which preferably includes a microcode based controller 100, an instruction sore module 30 (both shown in Figure 3 and an instruction decode module 20).

a7

Please replace the paragraph at page 12, lines 17-29 with the following paragraph

If, on the other hand, the test is of the board level type, a bit string in accordance with the IEEE 1149.1 standard is created, as indicated at 145, and an appropriate IEEE 1149.1 instruction is loaded into the instruction store module as instructions by applying an appropriate number of clock cycles, as indicated at 150. The bi t string is then applied to the test data interface (TDI), as indicated at 155 and the test access port (TAP) controller is set to the SHIFT-DR state, as indicated at 160 and an appropriate number of clock cycles are applied to transfer the bit string

a8

a8 into the instruction store module 30 as indicated at 165.